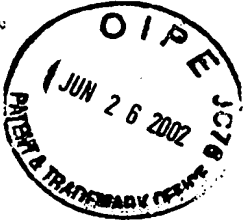


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re application of:

Khan *et al.*

Appl. No. 09/783,034

Filed: February 15, 2001

For: **Die-Down Ball Grid Array
Package with Die-Attached Heat
Spreader and Method for Making
the Same** (As Amended)

Confirmation No. 5713

Art Unit: 2826

Examiner: Andujar, L.

Atty. Docket: 1875.0210000

Information Disclosure Statement

Commissioner for Patents
Washington, D.C. 20231

Sir:

Listed on accompanying Form PTO-1449 are documents that may be considered material to the examination of this application, in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.56, 1.97 and 1.98.

Where the publication date of a listed document does not provide a month of publication, the year of publication of the listed document is sufficiently earlier than the effective U.S. filing date and any foreign priority date so that the month of publication is not in issue. Applicants have listed publication dates on the attached PTO-1449 based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicants reserve the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not

be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicants have checked the appropriate boxes below.

- ☐ 1. This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- ☒ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.
 - ☐ a. I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
 - ☐ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated

in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).

- ☒ c. Attached is our Check No. 35656 in the amount of \$ 180.00 in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 3. This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but before payment of the Issue Fee. Enclosed find our Check No. _____ in the amount of \$ _____ in payment of the fee under 37 C.F.R. § 1.17(p); in addition:
- ☐ a. I hereby state that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ 4. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. 1138 OG 37, 38.
- ☐ 5. A concise explanation of the relevance of the non-English language document(s) appears below:
- ☐ 6. Copies of the documents were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. _____, filed _____, which is relied upon for an earlier filing date under 35 U.S.C.

§ 120. Thus, copies of these documents are not attached. 37 C.F.R.
§ 1.98(d).

It is respectfully requested that the Examiner initial and return a copy of the enclosed PTO-1449, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.



Jeffrey S. Weaver
Attorney for Applicants
Registration No. 45,608

Date: 6-26-02

1100 New York Avenue, N.W.
Suite 600
Washington, D.C. 20005-3934
(202) 371-2600

FORM PTO-1449

ATTY. DOCKET NO.
1875.0210000APPLICATION NO.
09/783,034

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

APPLICANT
Khan et al.FILING DATE
February 15, 2001GROUP
2826

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	5,397,921	03/1995	Karnazos	257	779	
	AB1	5,474,957	12/1995	Urushima	437	209	
	AC1	5,534,467	07/1996	Rostoker	437	209	
	AD1	09/984,259	---	Zhao et al.	---	---	10/29/2001
	AE1	09/997,272	---	Zhao et al.	---	---	11/30/2001
	AF1	09/742,366	---	Khan et al.	---	---	12/22/2000
	AG1						
	AH1						
	AI1						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ1	EP 0 504 411 B1	06/1998	EPO	H01L	23/04	Yes No
	AK1						Yes No
	AL1						Yes No
	AM1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	1	Ahn, S.H. and Kwon, Y.S., "Popcorn Phenomena in a Ball Grid Array Package", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part B: Advanced Packaging, IEEE, August 1995, Vol. 18, No. 3, pp. 491-96.
	AO	1	Amkor Electronics, "Amkor BGA Packaging: Taking The World By Storm", Electronic Packaging & Production, Cahners Publishing Company, May 1994, page unknown.
	AP	1	Anderson, L. and Trabucco, B., "Solder Attachment Analysis of Plastic BGA Modules", Surface Mount International Conference, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 189-194.
	AQ	1	Andrews, M., "Trends in Ball Grid Array Technology," Ball Grid Array National Symposium, March 29-30, 1995, Dallas, Texas, 10 pages.
	AR	1	Attarwala, A.I. Dr. and Stierman, R., "Failure Mode Analysis of a 540 Pin Plastic Ball Grid Array", Surface Mount International Conference, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 252-257.

EXAMINER

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2826**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2						
	AB2						
	AC2						
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	AI2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ2						Yes No
	AK2						Yes No
	AL2						Yes No
	AM2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>2</u>	Banerji, K., "Development of the Slightly Larger Than IC Carrier (SLICC), Journal of Surface Mount Technology, July 1994, pp. 21-26.
	AO	<u>2</u>	Bauer, C., Ph.D., "Partitioning and Die Selection Strategies for Cost Effective MCM Designs", Journal of Surface Mount Technology, October 1994, pp. 4-9.
	AP	<u>2</u>	Bernier, W.E. et al., "BGA vs. QFP: A Summary of Tradeoffs for Selection of High I/O Components", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 181-185.
	AQ	<u>2</u>	Burgos, J. et al., "Achieving Accurate Thermal Characterization Using a CFD Code-- A Case Study of Plastic Packages", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE, December 1995, Vol. 18, No. 4, pp. 732-738.
	AR	<u>2</u>	Chadima, M., "Interconnecting Structure Manufacturing Technology," Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995.

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	AA3						
	AB3						
	AC3						
	AD3						
	AE3						
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	AG3						
	AH3						
	AI3						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ3						Yes No
	AK3						Yes No
	AL3						Yes No
	AM3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>3</u>	Chanchani, R. et al., "Mini BGA: Pad and Pitch Ease Die Test and Handling", Advanced Packaging, IHS Publishing Group, May/June 1995, pp.34, 36-37.
	AO	<u>3</u>	Chung, T.C. et al., "Rework of Plastic, Ceramic, and Tape Ball Grid Array Assemblies", Ball Grid Array National Symposium Proceedings, Dallas, Texas, March 29-30, 1995, pp. 1-15.
	AP	<u>3</u>	Cole, M.S. and Caulfield, T. "A Review of Available Ball Grid Array (BGA) Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 4-11.
	AQ	<u>3</u>	Cole, M.S. and Caulfield, T., "Ball Grid Array Packaging", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 147-153.
	AR	<u>3</u>	Dobers, M. and Seyffert, M., "Low Cost MCMs: BGAs Provide a Fine-Pitch Alternative", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 28, 30 and 32.

EXAMINER	DATE CONSIDERED
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2826**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4						
	AB4						
	AC4						
	AD4						
	AE4						
	AF4						
	AG4						
	AH4						
	AI4						

FOREIGN PATENT DOCUMENTS

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	AJ4						Yes No
	AK4						Yes No
	AL4						Yes No
	AM4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>4</u>	Dody, G. and Burnette, T., "BGA Assembly Process and Rework", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 39-45.
	AO	<u>4</u>	Edwards, D. et al., "The Effect of Internal Package Delaminations on the Thermal Performance of PQFP, Thermally Enhanced PQFP, LOC and BGA Packages", 45th Electronic Components & Technology Conference, IEEE, May 21-24, 1995, Las Vegas, NV, pp. 285-292.
	AP	<u>4</u>	Ejim, T.L. et al., "Designed Experiment to Determine Attachment Reliability Drivers for PBGA Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 30-38.
	AQ	<u>4</u>	Ewanich, J. et al., "Development of a Tab (TCP) Ball Grid Array Package", Proceedings of the 1995 International Electronics Packaging Conference, San Diego, CA, September 24-27, 1995, pp. 588-594.
	AR	<u>4</u>	Fausser, S. et al., "High Pin-Count PBGA Assembly", Circuits Assembly, February 1995, Vol 6, No. 2, pp. 36-38 and 40.

EXAMINER	DATE CONSIDERED
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U.S. PATENT DOCUMENTS

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	AA5						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ5						Yes No
	AK5						Yes No
	AL5						Yes No
	AM5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>5</u>	Fausser, Suzanne et al., "High Pin Count PBGA Assembly: Solder Defect Failure Modes and Root Cause Analysis", Surface Mount International, Proceedings of The Technical Program, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 169-174.
	AO	<u>5</u>	Ferguson, M. "Ensuring High-Yield BGA Assembly", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 54, 56 and 58.
	AP	<u>5</u>	Freda, M., "Laminate Technology for IC Packaging", Electronic Packaging & Production, Cahnners Publishing Company, October 1995, Vol. 35, No. 11, pp. S4-S5.
	AQ	<u>5</u>	Freedman, M., "Package Size and Pin-Out Standardization", Ball Grid Array National Symposium, March 29-30, 1995, 7 pages.
	AR	<u>5</u>	Freyman, B. and Pennisi, R., "Over-molded Plastic Pad Array Carriers (OMPAC): A Low Cost, High Interconnect Density IC Packaging Solution for Consumer and Industrial Electronics", 41st Electronic Components & Technology Conference, IEEE, May 11-16, 1991, pp. 176-82.

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APPLICANT
Khan et al.FILING DATE
February 15, 2008GROUP
2826

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6						
	AB6						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ6						No
	AK6						Yes No
	AL6						Yes No
	AM6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>6</u>	Freyman, B. et al., "Surface Mount Process Technology for Ball Grid Array Packaging", Surface Mount International Conference Proceedings, Surface Mount International, August 29-September 2, 1993, San Jose, California, pp. 81-85.
	AO	<u>6</u>	Freyman, B. et al., "The Move to Perimeter Plastic BGAs", Surface Mount International Conference Proceedings, San Jose, CA, August 29-31, 1995, pp. 373-382.
	AP	<u>6</u>	Freyman, B., "Trends in Plastic BGA Packaging," Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 45 pages.
	AQ	<u>6</u>	Gilleo, K., "Electronic Polymers: Die Attach and Oriented Z-Axis Films", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 37-38, 40 and 42.
	AR	<u>6</u>	Guenin, B. et al., "Analysis of a Thermally Enhanced Ball Grid Array Package", IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part A, IEEE Components, Packaging, and Manufacturing Technology Society, December 1995, Vol. 18, No. 4, pp. 749-757.

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2826**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA7						
	AB7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AJ7						Yes No
	AK7						Yes No
	AL7						Yes No
	AM7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	Z	Hart, C., "Vias in Pads for Coarse and Fine Pitch Ball Grid Arrays", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 203-207.
	AO	Z	Hart, C. "Vias in Pads", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 42, 44-46 and 50.
	AP	Z	Hattas, D., "BGAs Face Production Testing: New Package Offers Promise but Must Clear Technology Hurdles.", Advanced Packaging, IHS Publishing Group, Summer 1993, Vol. 2, No. 3, pp. 44-46.
	AQ	Z	Heitmann, R., "A Direct Attach Evolution: TAB, COB and Flip Chip Assembly Challenges", Advanced Packaging, IHS Publishing Group, July/August 1994, Vol. 3, No. 4, pp. 95-99 and 103.
	AR	Z	Hodson, T., "Study Examines BGA Use", Electronic Packaging & Production, March 1993, page unknown.

EXAMINER	DATE CONSIDERED
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
	AB8						
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	AH8						
	AI8						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ8						Yes No
	AK8						Yes No
	AL8						Yes No
	AM8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>8</u>	Holden, H., "The Many Techniques of Small Via Formation for Thin Boards", The Institute for Interconnecting and Packaging Electronic Circuits Ball Grid Array National Symposium, San Diego, CA, January 18-19, 1996, pp. 1-7.
	AO	<u>8</u>	Houghten, J., "New Package Takes On QFPs", Advanced Packaging, IHS Publishing Group, Winter 1993, Vol. 2, No. 1, pp. 38-39.
	AP	<u>8</u>	"How To Give Your BGAs A Better Bottom Line.", Advanced Packaging, IHS Publishing Group, January/February 1995, page unknown.
	AQ	<u>8</u>	Huang, W. and Ricks, J., "Electrical Characterization of PBGA for Communication Applications by Simulation and Measurement", National Electronic Packaging and Production Conference West '95, February 26-March 2, 1995, Anaheim, California, pp. 300-307.
	AR	<u>8</u>	Hundt, M. et al., "Thermal Enhancements of Ball Grid Arrays", National Electronic Packaging and Production Conference West '95, Reed Exhibition Companies, Anaheim, CA, February 25-29, 1996, pp. 702-711.

EXAMINER

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2826**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
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	AH9						
	AI9						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ9						Yes No
	AK9						Yes No
	AL9						Yes No
	AM9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	2	Hutchins, C.L., "Understanding Grid Array Packages", Surface Mount Technology Magazine, IHS Publishing Group, November 1994, Vol. 8, No. 11, pp. 12-13.
	AO	2	Hwang, J.S., "Reliability of BGA Solder Interconnections", Surface Mount Technology Magazine, IHS Publishing Group, September 1994, Vol. 8, No. 9, pp. 14-15.
	AP	2	Hwang, J.S., "A Hybrid of QFP and BGA Architectures", Surface Mount Technology Magazine, IHS Publishing Group, February 1995, Vol. 9, No. 2, p. 18.
	AQ	2	Johnson, R. et al., "A Feasibility Study of of Ball Grid Array Packaging", National Electronic Packaging and Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 413-422.
	AR	2	Johnson, R. et al., "Thermal Characterization of 140 and 225 Pin Ball Grid Array Packages", National Electronic Packaging & Production Conference East '93, Boston, Massachusetts, June 14-17, 1993, pp. 423-430.

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	AA10						
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	AI10						

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	AJ10						Yes No
	AK10						Yes No
	AL10						Yes No
	AM10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>10</u>	Johnston, P., "Land Pattern Interconnectivity Schemes", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, pages 2-21.
	AO	<u>10</u>	Johnston, P. "Printed Circuit Board Design Guidelines for Ball Grid Array Packages", Journal of Surface Mount Technology, Surface Mount Technology Association, January 1996, Vol. 9, pp. 12-18.
	AP	<u>10</u>	Kawahara, T. et al., "Ball Grid Array Type Package By Using of New Encapsulation Method", Proceedings of the 1995 International Electronics Packaging Conference, San Diego, CA, September 24-27, 1995, pp. 577-587.
	AQ	<u>10</u>	Knickerbocker, J.U. and Cole, M.S., "Ceramic BGA: A Packaging Alternative", Advanced Packaging, IHS Publishing Group, January/February 1995, Vol. 4, No. 1, pp. 20, 22 and 25.
	AR	<u>10</u>	Kromann, G., et al., "A Hi-Density C4/CBGA Interconnect Technology for a CMOS Microprocessor", National Electronic Packaging and Production Conference West '95, IEEE, February 26-March 2, 1995, Anaheim, California, pp. 1523-1529.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA11						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ11						Yes No
	AK11						Yes No
	AL11						Yes No
	AM11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>11</u>	Kunkle, R., "Discrete Wiring for Array Packages", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 9 pages.
	AO	<u>11</u>	Lall, B. et al, "Methodology for Thermal Evaluation of Multichip Modules", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE, December 1995, Vol. 18, No. 4, pp. 758-764.
	AP	<u>11</u>	Lasance, C. et al., "Thermal Characterization of Electronic Devices with Boundary Condition Independent Compact Models", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, IEEE Components, Packaging, and Manufacturing Technology Society, December 1995, Vol. 18, No. 4, pp. 723-731.
	AQ	<u>11</u>	Lau, J., "Ball Grid Array Technology", McGraw-Hill Inc., 1995, entire book submitted.
	AR	<u>11</u>	Lau, J. et al., "No Clean Mass Reflow of Large Plastic Ball Grid Array Packages", Circuit World, Wela Publications Ltd., Vol. 20, No. 3, March 1994, pp.15-22.

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FORM PTO-1449

ATTY. DOCKET NO.
1875.0210000APPLICATION NO.
09/783,034

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

APPLICANT
Khan et al.FILING DATE
February 15, 2008GROUP
2826

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA12						
	AB12						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ12						Yes No
	AK12						Yes No
	AL12						Yes No
	AM12						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	12	"Literature Review", Special Supplement to Electronic Packaging & Production, February 1995, Cahners Publication, 10 pages.
	AO	12	LSI LOGIC Package Selector Guide, Second Edition, LSI Logic Corporation, 1994-1995, entire document submitted.
	AP	12	"LTCC MCMs Lead to Ceramic BGAs," Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 14-15.
	AQ	12	Mak, Dr. W.C. et al., "Increased SOIC Power Dissipation Capability Through Board Design and Finite Element Modeling", Journal of Surface Mount Technology, Surface Mount International, October 1994, pp. 33-41.
	AR	12	Marrs, R.C. and Olachea, G., "BGAs For MCMs: Changing Markets and Product Functionality", Advanced Packaging, IHS Publishing Group, September/October 1994, Vol. 3, No. 5, pp. 48, 50, and 52.

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA13						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ13						Yes No
	AK13						Yes No
	AL13						Yes No
	AM13						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>13</u>	Matthew, L.C. et al., "Area Array Packaging: KGD in a Chip-Sized Package", Advanced Packaging, IHS Publishing Group, July/August 1994, pp. 91-94.
	AO	<u>13</u>	Mawer, A. et al., "Plastic BGA Solder Joint Reliability Considerations", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 239-251.
	AP	<u>13</u>	Mazzullo, T. and Schaertl, L., "How IC Packages Affect PCB Design", Surface Mount Technology Magazine, February 1995, Vol. 9, No. 2, pp. 114-116.
	AQ	<u>13</u>	Mearig, J., "An Overview of Manufacturing BGA Technology", National Electronic Packaging and Production Conference West '95, February 26-March 2, 1995, Anaheim, California, pp. 295-299.
	AR	<u>13</u>	Mertol, A., "Application of the Taguchi Method on the Robust Design of Molded 225 Plastic Ball Grid Array Packages", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part B: Advanced Packaging, IEEE, November 1995, Vol. 18, No. 4, pp. 734-743.

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2826**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA14						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ14						Yes No
	AK14						Yes No
	AL14						Yes No
	AM14						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>14</u>	Mescher, P. and Phelan, G., "A Practical Comparison of Surface Mount Assembly for Ball Grid Array Components", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 164-168.
	AO	<u>14</u>	Mulgaonker, S. et al., "An Assessment of the Thermal Performance of the PBGA Family", Eleventh Annual IEEE Semiconductor Thermal Measurement and Management Symposium, IEEE, San Jose, CA, February 7-9, 1995, pp. 17-27.
	AP	<u>14</u>	"New PBGA Pushes Technology to Outer Limits", Advanced Packaging, IHS Publishing Group, January/February 1995, page 11.
	AQ	<u>14</u>	Olachea, G., "Managing Heat: A Focus on Power IC Packaging", Electronic Packaging & Production (Special Supplement), Cahners Publishing Company, November 1994, pp. 26-28.
	AR	<u>14</u>	"Pad Array Improves Density", Electronic Packaging & Production, Cahners Publishing Company, May 1992, pp. 25-26.

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Khan et al.FILING DATE
February 15, 2001APPLICATION NO.
09/783,034GROUP
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA15						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ15						Yes No
	AK15						Yes No
	AL15						Yes No
	AM15						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>15</u>	Partridge, J. and Viswanadham, P., "Organic Carrier Requirements for Flip Chip Assemblies", Journal of Surface Mount Technology, Surface Mount Technology Association, July 1994, pp. 15-20.
	AO	<u>15</u>	Ramirez, C. and Fauser, S., "Fatigue Life Comparison of The Perimeter and Full Plastic Ball Grid Array", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September1, 1994, San Jose, California, pp. 258-266.
	AP	<u>15</u>	Rogren, P., "MCM-L Built on Ball Grid Array Formats", National Electronic Packaging and Production Conference West '94, Anaheim, California, pp. 1277-1282.
	AQ	<u>15</u>	Rooks, S., "X-Ray Inspection of Flip Chip Attach Using Digital Tomosynthesis", Surface Mount International, Proceedings of The Technical Program, August 28-September1, 1994, San Jose, California, pp. 195-202.
	AR	<u>15</u>	Rukavina, J., "Attachment Methodologies: Ball Grid Array Technology", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, 37 pages.

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

APPLICANT
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE
	AA16						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION
	AJ16						Yes No
	AK16						Yes No
	AL16						Yes No
	AM16						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>16</u>	Sack, T., "Inspection Technology", Ball Grid Array National Symposium, Dallas, Texas, March 29-30, 1995, pages 1-41.
	AO	<u>16</u>	Sakaguchi, H., "BGA Mounting Technology," pgs. 1-4, date and source unknown.
	AP	<u>16</u>	Schmolze, C. and Fraser, A., "SPICE Modeling Helps Enhance BGA Performance", Electronic Packaging & Production, January 1995, pp. 50-52.
	AQ	<u>16</u>	Semiconductor Group Package Outlines Reference Guide, Texas Instruments, 1995, entire document submitted.
	AR	<u>16</u>	Shimizu, J., "Plastic Ball Grid Array Coplanarity", Surface Mount International Conference, San Jose, California, August 31-September 2, 1993, pp. 86-91.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA17						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ17						Yes No
	AK17						Yes No
	AL17						Yes No
	AM17						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	17	Sigliano, R., "Using BGA Packages: An Appealing Technology in a QFP and Fine-Pitch Market", Advanced Packaging, IHS Publishing Group, March/April 1994, pp. 36-39.
	AO	17	Sirois, L., "Dispensing for BGA: Automated Liquid Dispensing in a High-Density Environment", Advanced Packaging, IHS Publishing Group, May/June 1995, pp. 38 and 41.
	AP	17	Solberg, V., "Interconnection Structure Preparation: Impact of Material Handling and PCB Surface Finish on SMT Assembly Process Yield", Ball Grid Array National Symposium, Dallas Texas, March 29-30, 1995, 10 pages.
	AQ	17	"Survival of the Fittest", Advanced Packaging, IHS Publishing Group, March/April 1995, page unknown.
	AR	17	Tuck, J., "BGA Technology Branches Out", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 24, 26, and 28.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA18						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ18						Yes No
	AK18						Yes No
	AL18						Yes No
	AM18						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>18</u>	"Tutorial and Short Courses", 45th Electronic Components & Technology Conference, May 21-24, 1995, Las Vegas, Nevada, IEEE, 6 pages.
	AO	<u>18</u>	Vardaman, E. J. and Crowley, R.T., "Worldwide Trends In Ball Grid Array Developments", National Electronic Packaging and Production Conference West '96, Reed Exhibition Companies, Anaheim, CA, February 25-29, 1996, pp. 699-701.
	AP	<u>18</u>	Walshak, D. and Hashemi, H., "Thermal Modeling of a Multichip BGA Package", National Electronic Packaging and Production Conference West '94, Reed Exhibition Companies, Anaheim, California, February 27-March 4, 1994, pp. 1266-1276.
	AQ	<u>18</u>	Walshak, D. and Hashemi, H., "BGA Technology: Current and Future Direction for Plastic, Ceramic and Tape BGAs", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 157-163.
	AR	<u>18</u>	Xie, H. et al., "Thermal Solutions to Pentium Processors in TCP in Notebooks and Sub-Notebooks", 45th Electronic Components & Technology Conference, IEEE, Las Vegas, NV, May 21-24, 1995, pp. 201-210.

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February 15, 2001APPLICATION NO.
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA19						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ19						Yes No
	AK19						Yes No
	AL19						Yes No
	AM19						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>19</u>	Yip, W.Y., "Package Characterization of a 313 Pin BGA", National Electronic Packaging and Production Conference West '95, Reed Exhibition Companies, February 26-March 2, 1995, Anaheim, California, pp. 1530-1541.
	AO	<u>19</u>	Zamborsky, E., "BGAs in the Assembly Process", Circuits Assembly, February 1995, Vol. 6, No. 2, pp. 60, 62-64.
	AP	<u>19</u>	Zimerman, M., "High Performance BGA Molded Packages for MCM Application", Surface Mount International Conference Proceedings, Surface Mount International, August 28-September 1, 1994, San Jose, California, pp. 175-180.
	AQ	<u>19</u>	Zweig, G., "BGAs: Inspect the Process, Not the Product", Electronic Packaging & Production (Special Supplement), Cahners Publishing Company, August 1994 (Supplement), p. 41.
	AR	<u>19</u>	Houghten, J.L., "Plastic Ball-Grid Arrays Continue To Evolve", Electronic Design, February 6, 1995, pp. 141-146.

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1875.0210000APPLICATION NO.
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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

APPLICANT
Khan et al.FILING DATE
SEPTEMBER 15, 2001GROUP
2826

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA20						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AJ20						Yes No
	AK20						Yes No
	AL20						Yes No
	AM20						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AN	<u>20</u>	Marrs, R. et al., "Recent Technology Breakthroughs Achieved with the New <i>SuperBGA®</i> Package", 1995 International Electronics Packaging Conference, San Diego, California, September 24-27, 1995, pp. 565-576.
	AO	<u>20</u>	Hayden, T.F. et al., "Thermal & Electrical Performance and Reliability Results for Cavity-Up Enhanced BGAs", Electronic Components and Technology Conference, IEEE, 1999, pp. 638-644.
	AP	<u>20</u>	Thompson, T., "Reliability Assessment of a Thin (Flex) BGA Using a Polyimide Tape Substrate", International Electronics Manufacturing Technology Symposium, IEEE, 1999, pp. 207-213.
	AQ	<u>20</u>	
	AR	<u>20</u>	

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